APPLICATION NOTE

Residual Phase Noise of Digital Frequency Dividers

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Many low noise synthesizers and phase-locked loops utilize frequency dividers to generate integer sub-multiple frequencies from available low noise sources. In order to preserve signal quality, it is desirable to use frequency dividers that exhibit the lowest residual noise properties. Since digital devices should suppress all AM noise, phase noise is of most interest. Residual phase noise measurements were made with similar devices from the four logic families of ECL, ACT, FAST and LS. Test conditions were held constant in order to provide comparative results. Test results indicate that ACT (CMOS) exhibits the lowest residual phase noise, followed by FAST, LS and ECL.

Introduction

The most common circuit used for digital frequency division consists of a series of bistable flip-flops with synchronous clock inputs. The synchronous frequency divider, shown in Figure 1, is considered more desirable than the asynchronous device. Noise present on the input signal causes the time at which the triggering signal crosses its threshold to vary, resulting in phase jitter ($\phi(t)$). In the synchronous frequency divider, the final output signal is dependent only on the jitter of the input signal, whereas in the asynchronous frequency divider, shown in Figure 2, the output signal jitter is dependent upon the noise of the input signal as well as the noise in all intermediate stages.

In most applications, specifications are provided in terms of signal phase noise spectral density $S_\phi(f_m)$ (the Fourier transform of $\phi(t)$) or single-sided phase noise $\mathcal{L}(f_m)$ where

$$N = 2^n$$

$$\mathcal{L}(f_m) = \frac{S_\phi(f_m)}{2}$$

$$S_{\phi out}(f_m) = \frac{S_{\phi in}(f_m)}{N^2}$$

which indicates the input phase noise should be reduced by a factor of N^2 (or 20*log(N) dB) for ideal frequency division. Due to the limitations of the physical electronics, there is an inherent limit to the output phase noise power spectral density ($S\phi(f_m)_{min}$). Consequently, when using digital frequency dividers in low noise applications, where the phase noise of the input clock is considerably lower than that of the electronics in the frequency dividers, the 20*log(N) rule is invalid. At best, one can expect output signal phase noise to be equal to the frequency divider limit ($S_\phi(f_m)_{min}$).

All logic families provide devices suitable for frequency division. Four logic families were chosen to be representative of the most likely candidates for applications in which a choice exists, that is, high frequency applications ($f_{in} > 100$ MHz) dictate the use of ECL. The families tested were ECL, FACT (Fairchild advanced CMOS with TTL outputs), FAST (Fairchild advanced Schottky barrier TTL) and LS (low power Schottky barrier TTL).

Description

In order to characterize each logic family accurately, an effort was made to keep all measurement parameters constant (frequency, amplitude, layout and independent noise contributors). In all cases (ECL and TTL), a synchronous +4 circuit was constructed. Due to the compatibility among TTL families, the same test fixture was used for LS, ACT and FAST devices. In this case, the test circuit consisted of two D-flip-flops (XX74s). The ECL test employed a 10H016 four-bit binary counter setup to pre-load a 12 (decimal). Consequently, only the first two of the four flip-flops contained in the counter were active, resulting in a circuit equivalent to the TTL +4. The TTL divider test

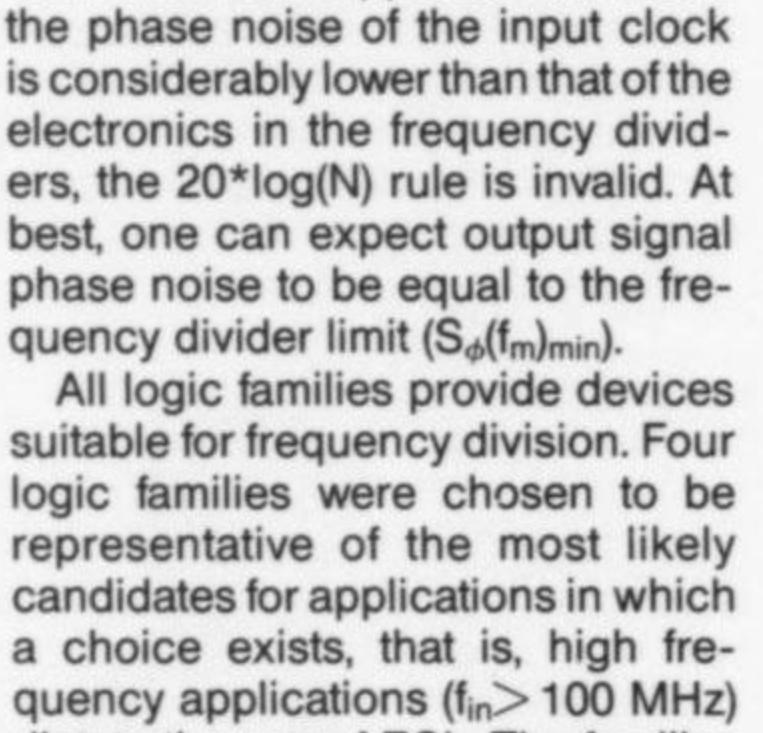

Fig. 1 The synchronous frequency divider.

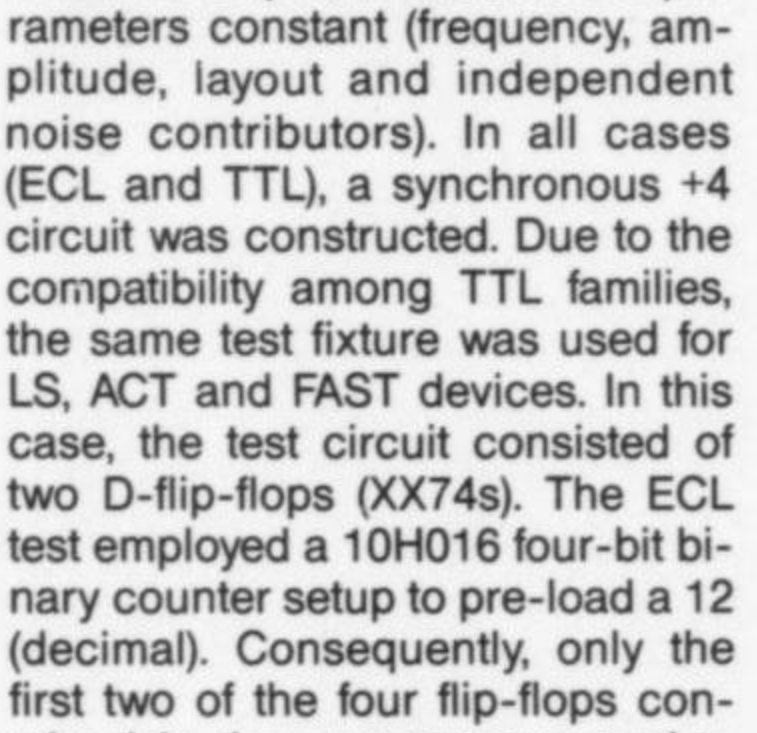

Fig. 2 The asynchronous frequency divider.

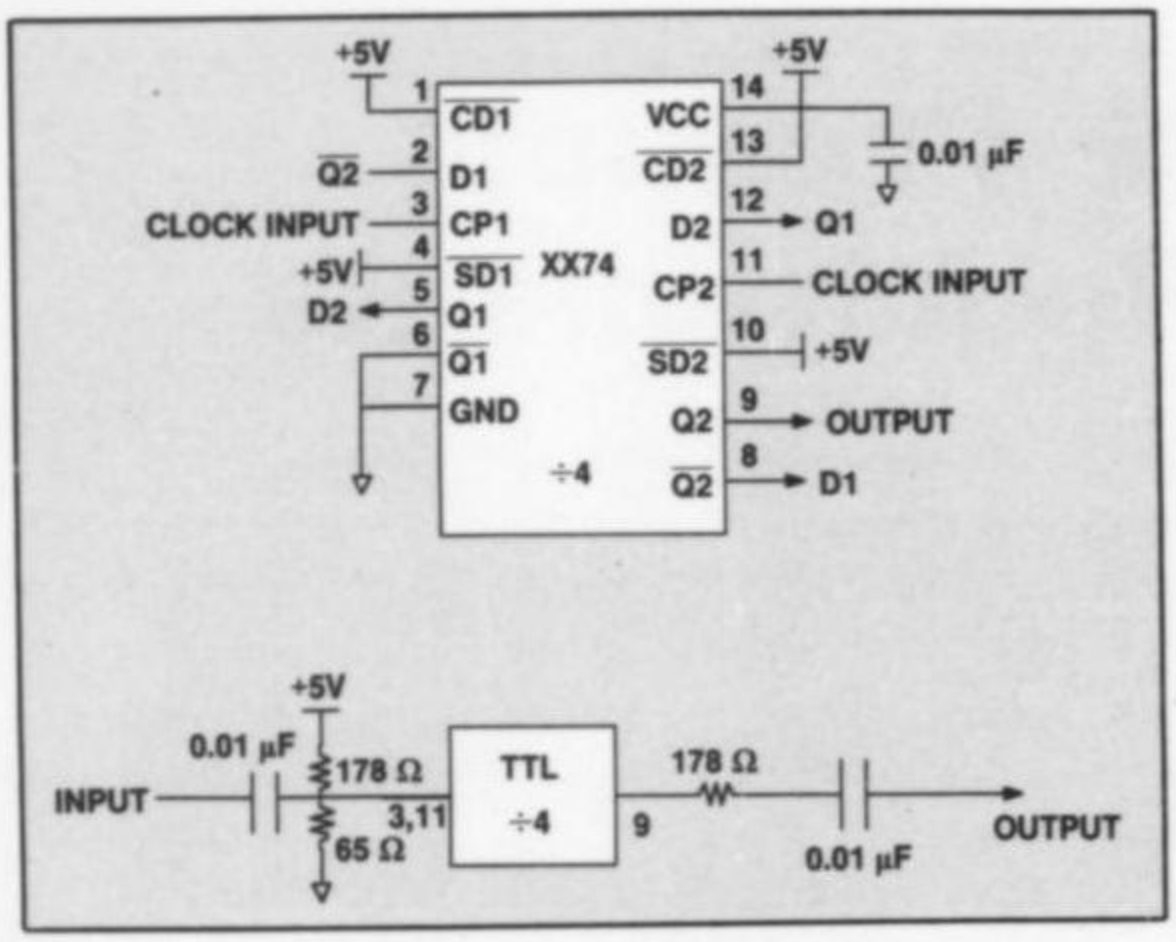

Fig. 3 The TTL frequency divider test fixture.

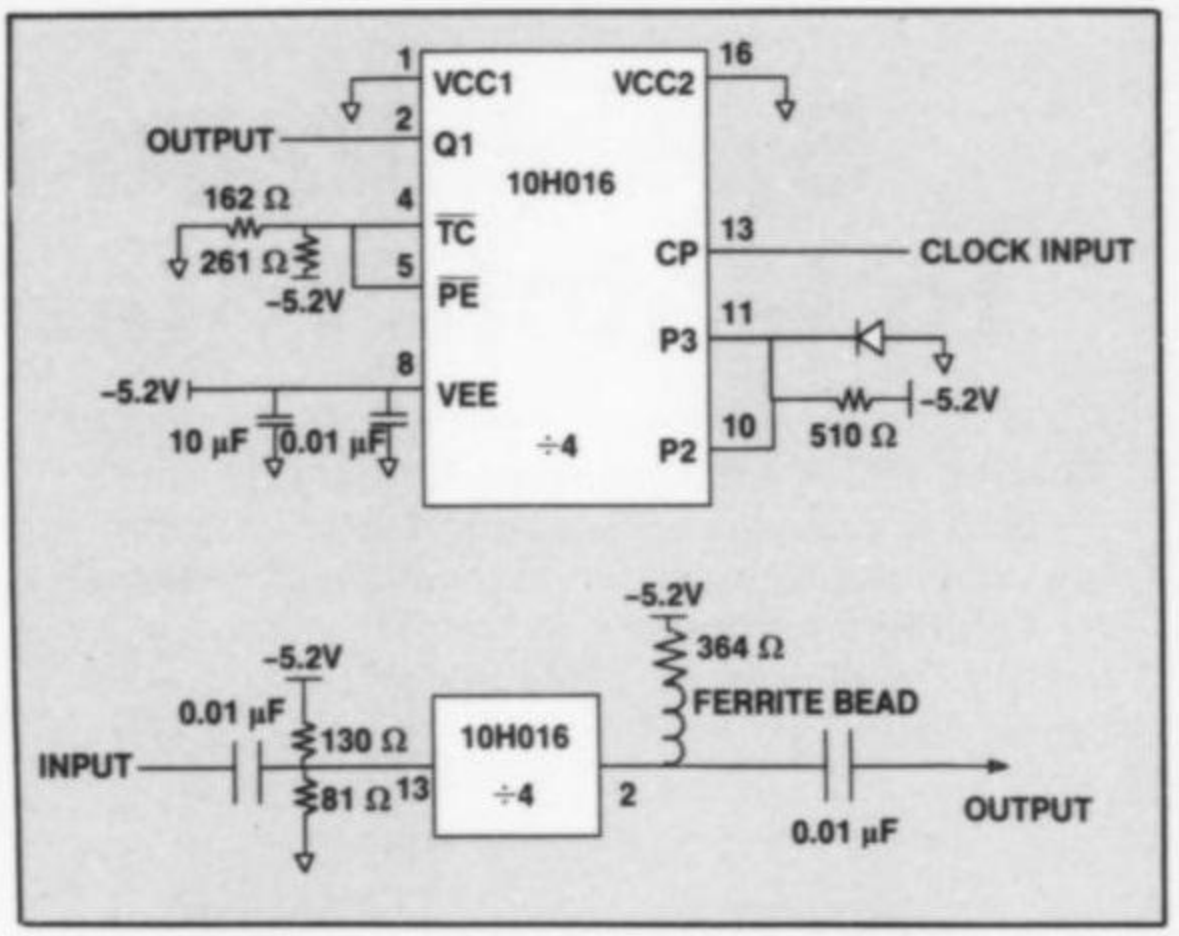

Fig. 4 An ECL frequency divider test fixture.

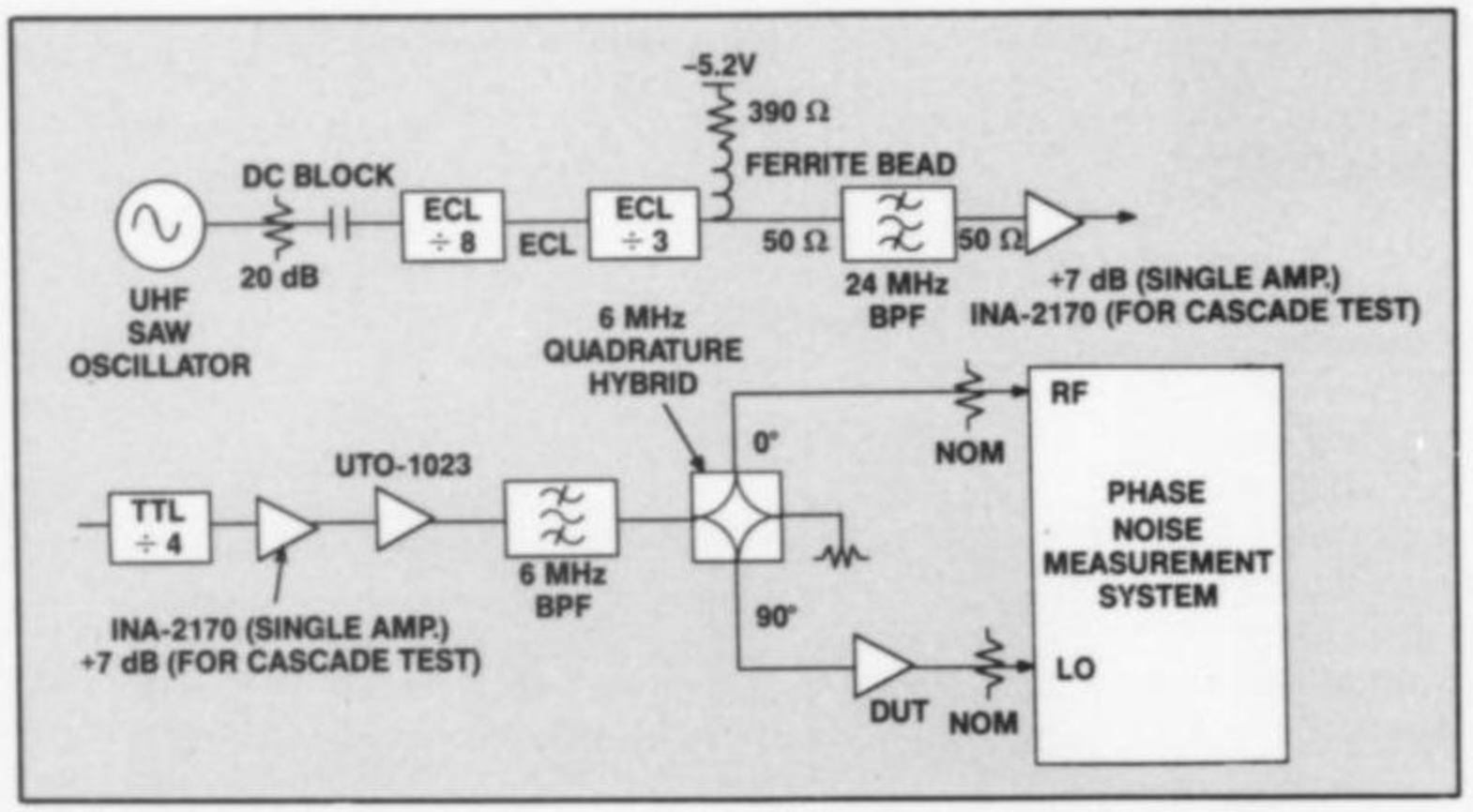

Fig. 5 The amplifier noise measurement setup.

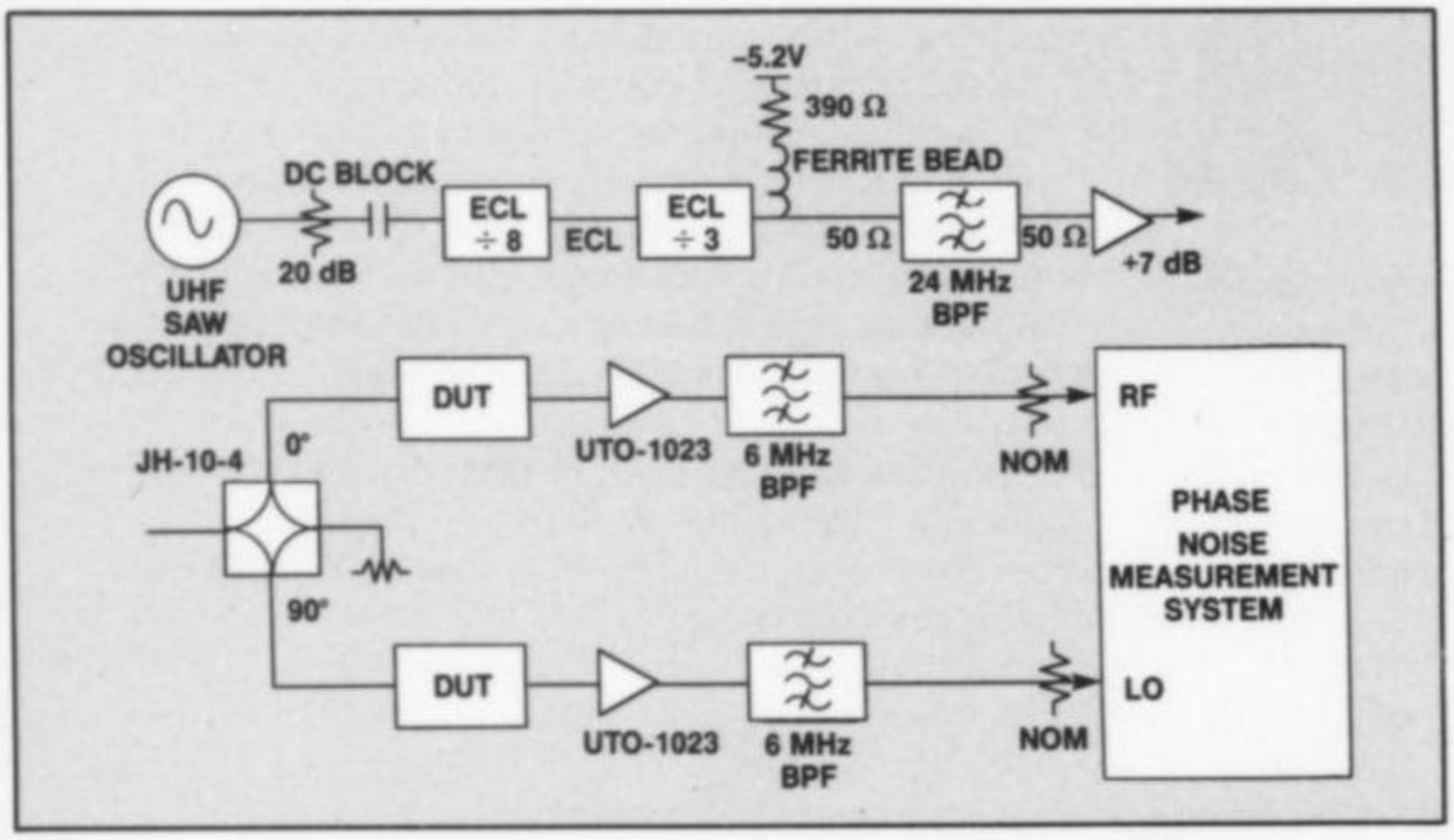

Fig. 6 A TTL frequency divider noise measurement setup.

fixture is shown in Figure 3 and the ECL divider test fixture is shown in Figure 4.

Figures 5, 6 and 7 show the setups used to make residual noise measurements. The theory of operation is that the phase noise of the signal applied to the input of the quadrature hybrid is common to both the RF and LO signal paths. Residual noise produced by devices in both the RF and LO paths is independent of any other device. Only active devices (amplifiers and frequency dividers) generate phase noise. Assuming the residual noise of the amplifiers in the independent paths is sufficiently low, the noise measured at the phase detector output consists only of the residual noise of each frequency divider. Assuming the frequency divider noise is independent and the two frequency dividers are essentially equal, the measured noise represents twice the noise power spectral density of a single frequency divider, that is, the desired data $\mathcal{L}(f_m)$, is 3 dB less than the measured data.

Results

Test results have been extracted from the measured data, shown in Figure 8. As illustrated, the ACT (CMOS) device exhibits the lowest residual noise, followed by FAST, LS and ECL. These results are consistent with intuition considering CMOS devices have the greatest signal swing (≈5 V), whereas ECL outputs undergo only a 1 V transition between states. Consequently, one would expect CMOS to have the greatest signal-to-noise ratio.

Residual noise consists of two basic phenomena, the first being additive or white noise. In this case, noise is added to the input signal in a linear fashion, which is the primary contributor to the noise floor (large f_m). The second noise mechanism is multiplicative or modulation noise. In this case, the input signal undergoes modulation by a $1/f_m$ spectral density. Considerably less is understood about the sources of multi-

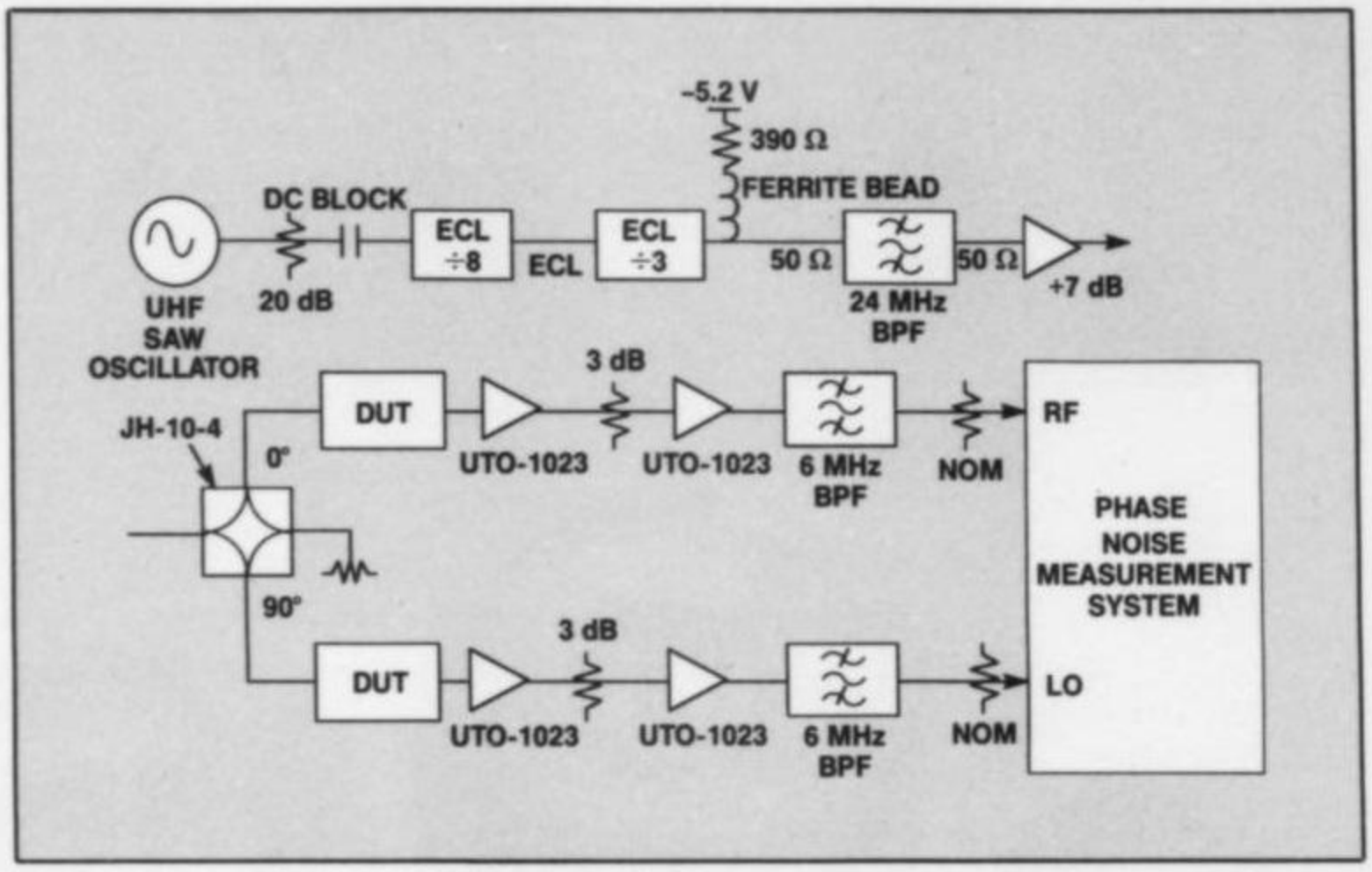

Fig. 7 An ECL frequency divider noise measurement setup.

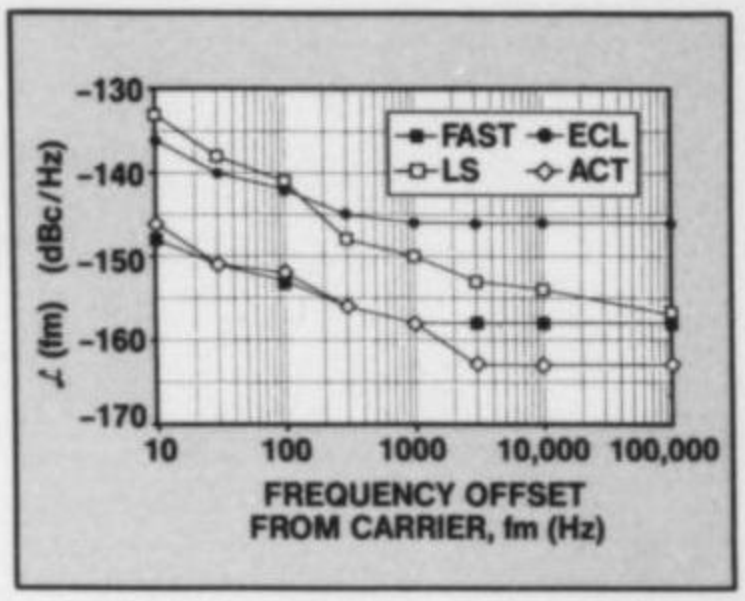

Fig. 8 Digital frequency divider residual phase noise.

plicative noise in comparison with additive noise. Multiplicative noise is the primary phase noise contributor at lower modulation frequencies. The frequency at which the two regions are divided is commonly referred to as the flicker frequency.

Table 1 lists the measured data and some theoretical predictions for residual phase noise. Egan's model[1] is the most complete and agrees closely with the measured data. Robins provides an estimate of additive noise (floor) only, whereas Kroupa and Egan provide a model for both multiplicative and additive noise.[1] Robins' estimate is much lower than the measured data, which is attributed to the fact that Robin's estimate represents a limit (minimum) given ideal component and test conditions.

TABLE I
MEASURED DATA

	ℒ (fm) dBc/Hz*				
	fm=10 Hz	fm=1.5 kHz	fm=100 kHz	Flicker Frequency	Data Set
ECL	-136	-146	-146	290 Hz	Measured
	—	-157	-157		Robins
	-138	-149	-153		Kroupa
	—	-143.7	-143.7		Egan
FAST	-148	-158	-158	900 Hz	Measured
	—	-170	-170		Robins
	-138	-149	-153		Kroupa
LS	-133	-151	-157	3 kHz	Measured
	—	-170	-170		Robins
	-138	-149	-153		Kroupa
ACT	-146	-159	-163	3 kHz	Measured
	-138	-149	-153		Kroupa

*ℒ = 1/2 signal phase noise spectral density

a function of output frequency, division ratio and input power level. Thus the data provided serves only as comparative study and is not an absolute measure of the residual noise to be encountered under varied circuit conditions.

Conclusion

The measured data clearly indicates ACT (CMOS) to be the family of choice for low noise frequency divider circuits. Unfortunately, input clock frequencies for this logic family are not specified beyond 85 MHz for military and 125 MHz for commercial applications. In high frequency applications, ECL is the only alternative. Residual phase noise is

Acknowledgment

The author would like to thank Philip Sullivan, principal engineer, Raytheon Co., for his constant support and technical guidance throughout the duration of this study. ■

References

1. W.F. Egan, "Modeling Phase Noise In Frequency Dividers," IEEE Trans. On Ultrasonics, Ferroelectrics and Frequency Control, Vol. 37, No. 4, July 1990, pp. 307–315.
2. T.R. Faulkner and R.E. Temple, "Residual Phase Noise and AM Noise Measurements and Techniques," Hewlett-Packard Inc.

Mark R. McClure *received his BSEE from Northeastern University in June 1990. Currently, he is pursuing his MSEE at Polytechnic University. He is a member of the technical staff at Raytheon Missile Systems Division, Missile Guidance Laboratory, Advanced Missiles Department, Exciter and Special Devices Section. His research interests are low noise, high stability microwave synthesizers, residual noise measurement and characterization, direct digital synthesizers and low noise phase lock loops.*