LNDIV
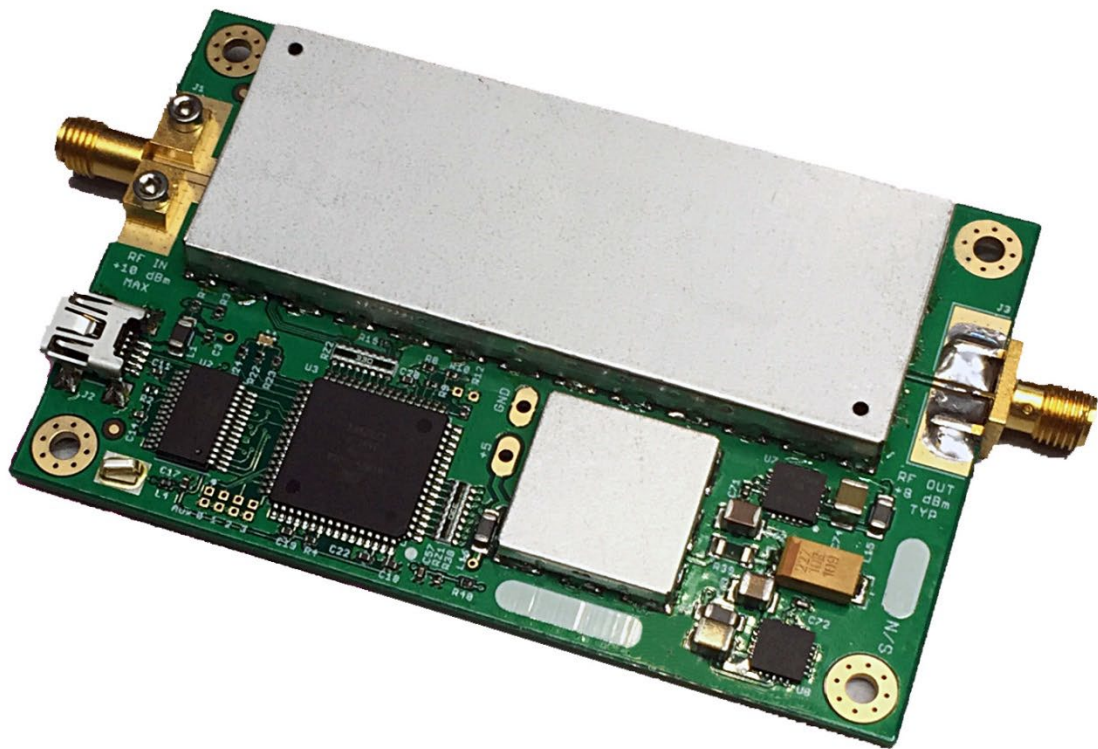
Operation and Programming

Miles Design LLC
16430 57th Ave SE
Snohomish, WA 98296
john@miles.io

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Functional Overview
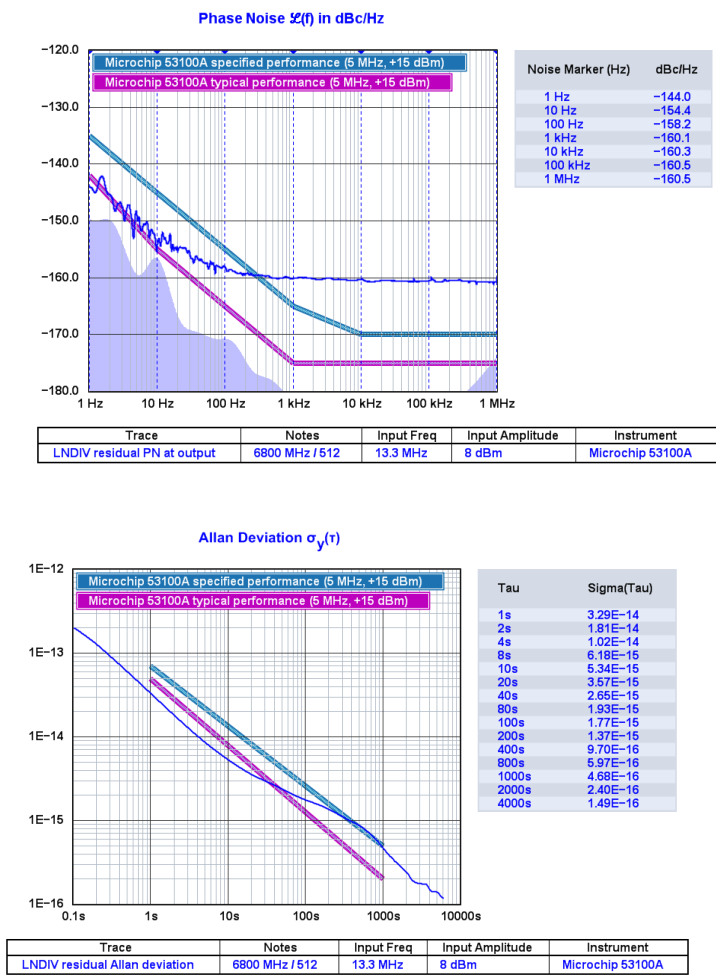
The LNDIV module provides frequency division of RF input signals between 100 MHz and 24 GHz by factors of 64 and higher. Input power levels between -5 and +10 dBm are supported, yielding typical output levels near +8 dBm. The module can be configured easily using a terminal program, with DC power sourced from the host USB connection or an external +5V supply for standalone operation.

Although capable of service as a general-purpose microwave frequency divider, the LNDIV module is designed primarily to support test and measurement applications that require exceptionally low levels of additive phase noise at close-in offsets. When employed as a frequency range extension module for the Microchip 53100A Phase Noise Analyzer, for example, LNDIV provides additive noise performance comparable to the instrument's own measurement floor at offsets near the output signal's carrier frequency.

Phase Noise 𝓛(f) in dBc/Hz

Noise Marker (Hz)	dBc/Hz
1 Hz	−144.0
10 Hz	−154.4
100 Hz	−158.2
1 kHz	−160.1
10 kHz	−160.3
100 kHz	−160.5
1 MHz	−160.5

Trace	Notes	Input Freq	Input Amplitude	Instrument
LNDIV residual PN at output	6800 MHz / 512	13.3 MHz	8 dBm	Microchip 53100A

Allan Deviation $\sigma_y(\tau)$

Tau	Sigma(Tau)
1s	3.29E−14
2s	1.81E−14
4s	1.02E−14
8s	6.18E−15
10s	5.34E−15
20s	3.57E−15
40s	2.65E−15
80s	1.93E−15
100s	1.77E−15
200s	1.37E−15
400s	9.70E−16
800s	5.97E−16
1000s	4.68E−16
2000s	2.40E−16
4000s	1.49E−16

Trace	Notes	Input Freq	Input Amplitude	Instrument
LNDIV residual Allan deviation	6800 MHz / 512	13.3 MHz	8 dBm	Microchip 53100A

For details on the use of the LNDIV module with the Microchip 53100A, please refer to Application Note AN3899, UHF and Microwave Measurements with the 53100A Phase Noise Analyzer.

Specifications

Operational limits and typical performance figures are shown below. Unless otherwise noted, phase noise and stability specifications are based on the default LNDIV settings (division by 512 with PRE=2, MAIN=128, and POST=2) with a 6800 MHz test signal at the maximum rated input power of +10 dBm.

Input frequency range	100 MHz – 24 GHz
Input signal level	-5 dBm to +10 dBm
Minimum division ratio	64
Maximum division ratio	>10,000 (limited by AC coupling components)
Division step size (default)	4
Output power	+8 dBm, AC coupled
Input impedance	50 ohms, VSWR < 3:1 through 18 GHz
Additive phase noise, output referred (1 Hz)	< -142 dBc/Hz
Additive phase noise, output referred (100 Hz)	< -157 dBc/Hz
Additive phase noise, output referred (1 kHz – 1 MHz)	< -160 dBc/Hz
Residual phase stability (1 hour warmup)	< ±3 ps/hour
Residual Allan deviation (t=1s)	< 4E-14
Residual Allan deviation (t=1000s)	< 1E-15
DC supply	+5V, < 600 mA
Dimensions (LxWxH)	11 cm x 6 cm x 1 cm
Ambient temperature	15C to 35C operating, -20C to +50C storage
RF connectors	2x SMA female

Operating Guidelines

While the LNDIV module is easy to use, the hints and tips below will help you take full advantage of its performance capabilities.

- Keep in mind that the LNDIV output is a square wave with strong harmonics that can extend beyond 1 GHz. When used with the Microchip 53100A or other equipment that expects a sinusoidal input signal, it is necessary to use an external lowpass filter at the instrument input such as the SLP-23 provided with each LNDIV module. Otherwise, spur performance may be impaired, or the instrument may fail to detect the input signal altogether. The lowpass filter should provide at least 30 dB of attenuation at the third harmonic of the anticipated output frequency.

- LED1 is an RGB LED that serves as a power-on self-test indicator. Following application of DC power, the LED should change from blue to green within approximately 3-4 seconds, indicating that the supply voltage is within range and that the controller can communicate with the divider hardware. If the LED turns red, insufficient power supply current is the most likely cause.

- The LNDIV module requires approximately 500 mA at +5 volts for operation. This current level will equal or slightly exceed the specified USB 2.0 power delivery limit of 500 mA. In most cases this will not be a problem, but some PCs, especially smaller laptops, may not supply enough voltage through their USB ports for reliable operation. As a result, if the LED on the LNDIV PCB changes from blue to red a few seconds after USB power is applied -- or if it goes out entirely -- you will need to use a higher-powered USB hub, a shorter USB cable, or both.   **Passive USB hubs and extension cables should not be used to supply power to the LNDIV module.**

- For best results when powering the LNDIV module from USB, use the 6' USB cable supplied (Tripp-Lite U030-006). This cable uses 24 AWG conductors for power and ground, rather than the more common 28 AWG or smaller wires.

- To configure the LNDIV board for use with external +5V power, **ferrite bead L16 must be removed**. Otherwise the external power supply will backfeed +5V to the USB hub or host PC if it is powered down with the LNDIV board connected. Additionally, **a 0-ohm 0402 jumper or solder bridge should be installed at R2** when using external power. The external power source should be connected to the large vias adjacent to L16 as indicated on the PCB silkscreen.

- Signals applied to the LNDIV module pass through a chain of three divider ICs. The overall division ratio achieved by the LNDIV module is simply the product of these ICs' individual division ratios. These stages are the prescaler (PRE) that allows input signals up to 24 GHz to be handled, the MAIN divider that contributes the bulk of the overall division ratio, and the POST divider that reclocks the MAIN divider's output signal and establishes a 50% output duty cycle.

- Under most circumstances, the SCPI DIV[:MODulus] command will be sufficient to configure the LNDIV module for the desired division ratio by selecting an appropriate setting for the MAIN divider based on the currently-selected PRE and POST division ratios. If the requested overall division ratio is unachievable, the resulting error message will include further information. The DIV[:MODulus] factor is preconfigured to 512 by default.

- The individual dividers (PRE, MAIN, and POST) whose factors make up the overall LNDIV division ratio may be programmed independently if required, using the SCPI commands PRE[:MODulus], MAIN[:MODulus], and POST[:MODulus], respectively.   However, it is recommended that the POST divider remain at its default setting of 2 at all times. The default setting provides an output duty cycle close to 50% regardless of the overall division ratio, achieving the optimum output power level (and thus SNR.)

- In addition to adjusting the MAIN and POST division factors independently through the SCPI command interface, it is also possible to configure the PRE divider for division ratios of 1, 2, 4, or 8. Empirically, the combination of ratios that yields the default overall division ratio of 512 with minimal additive noise appears to be PRE=2, MAIN=128, and POST=2. These are the settings chosen for the LNDIV board's factory defaults. Setting the PRE division ratio to 1 increases the additive noise slightly, while values of 4 or 8 have little or no effect on performance but will increase the minimum available step size for the board's overall division ratio.

- Because the input frequency at the MAIN divider (HMC983) is limited to 7 GHz, **note that the PRE divider ratio must be manually set to 4 or 8 to support input frequencies above 14 GHz.**

- In critical applications, be sure to measure the residual performance of the LNDIV module(s) at the operating frequency and division ratios required.   Not all division ratios supported by the MAIN divider will yield noise and spur levels similar to those observed at the default (512x) overall division setting; some will be substantially better than others.

- Normal operating temperature at the PCB surface will be very warm to the touch, approximately 40C to 50C. Use caution when positioning the LNDIV module near temperature-sensitive components or interconnects.

- Although the HMC862A prescaler IC (U1) is rated for use at input frequencies down to 100 MHz, residual noise and spur performance is likely to be degraded at frequencies under 650 MHz unless input signals with high input power levels and/or fast slew rates are applied.   For applications at these frequencies, consider using an external clock shaper.

- When using the SCPI command interface to configure the LNDIV module's operating parameters, **don't forget to issue a *SAV command** to write the new settings to EEPROM. Otherwise, any changes made will be lost at the next power cycle.

Connecting to the LNDIV Module

The LNDIV module supports serial communications through a USB-based "virtual COM port," using device drivers that are available for most operating systems at the FTDIChip website.   If your PC does not recognize the LNDIV module automatically, please refer to the instructions provided at https://ftdichip.com/drivers/vcp-drivers/ to install the current VCP driver for your system.

Almost any standard terminal program can be used to communicate with the LNDIV module. After you have installed the FTDIChip drivers and identified the virtual COM port associated with the module, you can use almost any terminal program to connect to the port. JLTerm offers built-in support for communication with SCPI-based instruments; some popular full-featured options include Tera Term and PuTTY.

Parameters such as baud rate and flow control may be set to any value, but local echo should normally be disabled. These connection details are handled automatically by JLTerm, which also displays a list of ports that is updated automatically when devices are connected and removed:
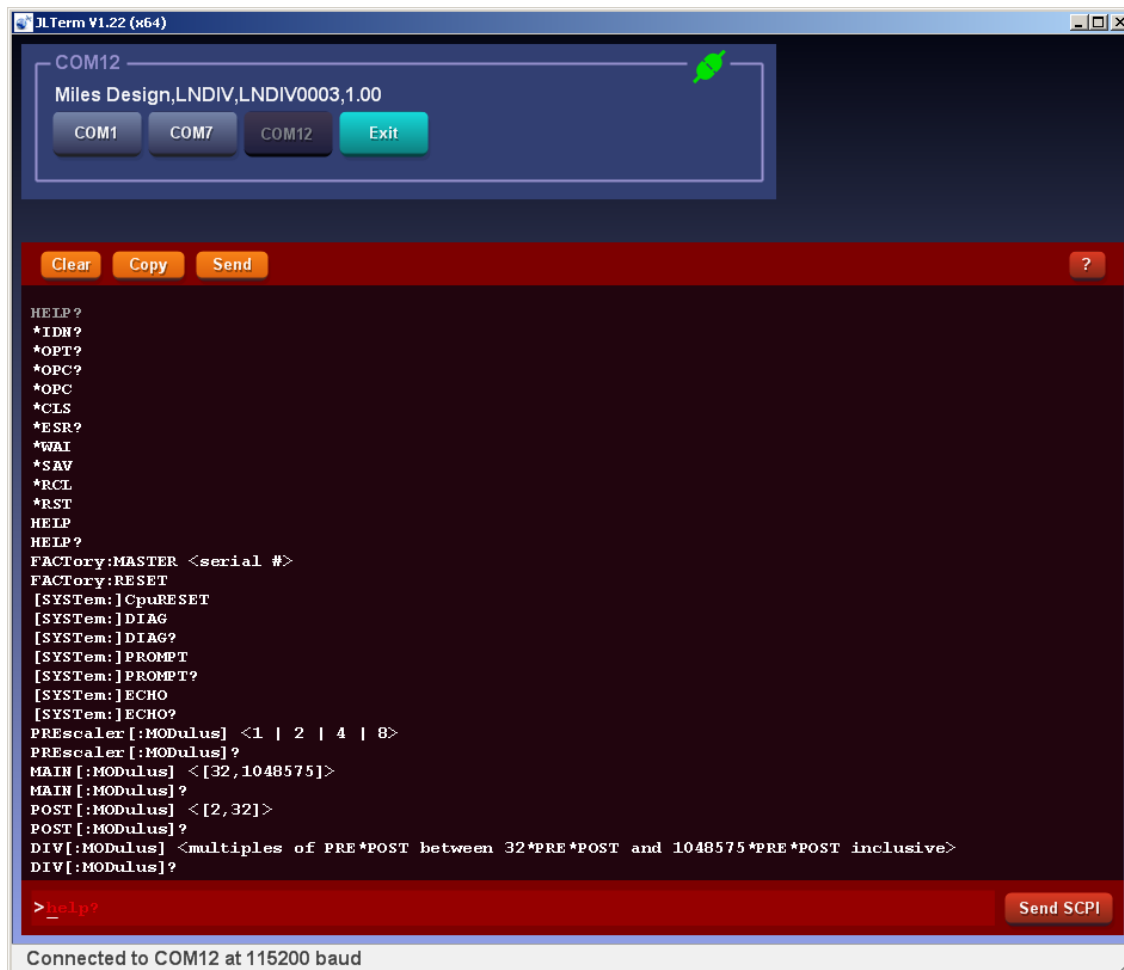
SCPI Command Guide

Communication with the LNDIV module takes place using a hierarchical command language whose syntax is based on IEEE 488.2 / SCPI guidelines. The complete list of commands and queries supported by the LNDIV firmware is provided here for reference.

Syntax and grammar conventions supported by the LNDIV module's SCPI firmware include the following:

- Portions of command and parameter definitions within square **[ ]** brackets are optional
- For both command and parameter descriptions, text in lowercase is also optional and may be omitted in whole or in part
- Commands and parameters are case-insensitive
- Hexadecimal values for integer parameters may optionally be specified with **0x** or **#H** prefixes
- Binary values for integer parameters may be specified with **0b** or **#B** prefixes
- Selected integer parameters accept **MIN** and **MAX** keywords as well as literal numeric values
- Commands with boolean parameters accept **1**, **0**, **On**, **Off**, **True**, or **False**
- Default values for enumerated parameters are underlined in the documentation when applicable

IEEE 488.2 Common Commands

The LNDIV frequency divider module supports the following subset of IEEE 488.2 Common Commands, as defined in Chapter 10 of IEEE Standard 488.2-1992.

In addition to the commands listed below, the command **HELP**[**?**] will return a list of all available SCPI commands.

*CLS

> Resets the Event Status register bits to zero.

*ESR?

> Returns and clears the current Event Status register value.
>
> > **Bit 0**: *OPC status (Operation complete)
> > **Bit 1**: Not used
> > **Bit 2**: Set when SCPI query error has been logged
> > **Bit 3**: Set when hardware fault has been logged
> > **Bit 4**: Set when SCPI execution error has been logged
> > **Bit 5**: Set when SCPI command error has been logged
> > **Bit 6**: Not used
> > **Bit 7**: Set at power on

*IDN?

Returns a string identifying the product, manufacturer, serial number, and firmware version of the connected hardware. For the LNDIV module, *IDN? returns a string of the form

```
Miles Design,LNDIV,LNDIV0003,1.00
```

*OPC?

Returns "1" when all pending operations are complete.

The LNDIV module does not support asynchronous command execution, so *OPC? always returns "1".

Appending the string **;*OPC?** to transmitted SCPI command lines is a convenient way to maintain synchronization of the LNDIV module's onboard SCPI command processor with external application software. It effectively turns any command into a query that will block the application's execution until the module is ready to receive further commands.

Note that the "1" result is returned after any concatenated commands have been executed, regardless of whether the *OPC? query appears at the end of the command list or elsewhere within it.

*OPC

This command sets bit 0 in the Event Status register when all pending operations are complete. As with *OPC?, the command form of *OPC has no meaningful effect on the LNDIV module.

*OPT?

Returns a list of hardware options present. Currently always returns "0".

*RCL

Forces immediate recall of the power-up state that was most recently stored with a *SAV command.

*RST

Resets the hardware state to its factory-default settings. **The *RST command does not affect stored power-up state information; it must be followed by *SAV to return the power-up settings to their factory defaults.**

Note that *RST does not physically reset the LNDIV module's CPU or any other internal hardware.   The SYSTem:CpuRESET command can be used for this purpose.

*SAV

Writes the current hardware control state to nonvolatile memory. The saved state will be restored in subsequent power-up cycles.

For optimum reliability and service life, **write operations to nonvolatile memory are performed by the LNDIV firmware only in response to an explicit *SAV command.** It is safe to cycle or interrupt power to the LNDIV module at any time when the *SAV command is not being processed.

*WAI

The standard SCPI *WAI command has no effect on the LNDIV module, since it is always in 'Operation Complete Idle' state.

System-Level Commands

FACTory:MASTER <serial #>

This command is used to write initial values including the serial number to EEPROM. It should not normally be issued at the user level.

FACTory:RESET

Same as *RST.

[SYSTem:]CpuRESET

Causes an immediate reboot of the LNDIV module's onboard microcontroller. All hardware registers are initialized, and all operating parameters are loaded from EEPROM, exactly as if a power cycle had occurred.

[SYSTem:]DIAG
[SYSTem:]DIAG?

Displays diagnostic information for the LNDIV module including estimated uptime, internal
supply voltage, and other parameters.

[SYSTem:]ECHO <bool>
[SYSTem:]ECHO?

Enables, disables, or queries the current remote echo setting. Remote echo is enabled by
default.

[SYSTem:]PROMPT <bool>
[SYSTem:]PROMPT?

Enables, disables, or queries the current setting for the SCPI text prompt ("**LNDIV SCPI > **"). The
SCPI prompt is enabled by default.

Divider Programming Commands

DIV[:MODulus] <ratio>
DIV[:MODulus]?

The DIV[:MODulus] command, abbreviated DIV, programs the MAIN divider (HMC983) to achieve the requested overall division ratio for the LNDIV module.

The following procedure is used by the DIV command:

1) Compute the overall division ratio step size as the product of the current PRE and POST division factors. (By default, both the PRE and POST divider stages are configured to divide by 2.)

2) Compute the minimum supported division ratio by multiplying the step size by the smallest supported MAIN divisor (32).

3) Compute the maximum supported division ratio by multiplying the step size by the largest supported MAIN divisor (2^20-1, or 1048575).

4) If the requested <ratio> is outside the limits computed above, or if it is not an integer multiple of the step size, issue an appropriate error message.

5) Program the MAIN divider to the specified <ratio> divided by the step size.

As a result, the MAIN divider is programmed such that that the product of PRE * MAIN * POST is equal to the user's specified <ratio>.

Note that when the query DIV:[MODulus]? is executed, the response is the *current* product of PRE * MAIN * POST, not the result of the last DIV:[MODulus] command.

MAIN[:MODulus] <ratio>
MAIN[:MODulus]?

The MAIN[:MODulus] command, abbreviated MAIN, programs the MAIN divider (HMC983) to achieve the specified division ratio for that stage. An error message is returned if the <ratio> parameter is outside the range [32,1048575].

The MAIN:[MODulus]? query, abbreviated MAIN?, returns the most recent value used to program the MAIN divider, regardless of whether it was established with a MAIN:[MODulus] or a DIV:[MODulus] command.

In most cases, the DIV:[MODulus] command should be used to program the MAIN divider, as it automatically computes the value required to achieve an overall division ratio based on the current PRE and POST divisors.

By default, the MAIN division ratio is 128, the PRE division ratio is 2, and the POST division ratio is 2, for an overall division ratio of 512.

POST[:MODulus] <ratio>
POST[:MODulus]?

The POST[:MODulus] command, abbreviated POST, programs the POST divider (HMC394) to achieve the specified division ratio for that stage. The default POST ratio is 2.

The POST:[MODulus]? query, abbreviated POST?, returns the most recent value used to program the POST divider.

Valid ratios for the POST divider range from 2 to 32 inclusive. Setting the POST division ratio to any value other than 2 is not recommended, as doing so will establish a suboptimal duty cycle and reduce the output SNR.

PRE[:MODulus] { 1 | 2 | 4 | 8 }
PRE[:MODulus]?

The PRE[:MODulus] command, abbreviated PRE, programs the prescaler (HMC862A) to achieve the specified division ratio for that stage.

The PRE:[MODulus]? query, abbreviated PRE?, returns the most recent value used to program the prescaler.

The selection of valid prescaler ratios is limited to 1, 2, 4, or 8.   The default PRE ratio of 2 represents a good compromise between SNR performance (which may be degraded slightly when the prescaler ratio is set to 1) and the minimum overall division step size (which is equal to the product of the PRE and POST division ratios.)

The output of the prescaler stage drives the MAIN divider (HMC983), whose specified input frequency is limited to a maximum of 7 GHz. Consequently, when it is necessary to use the LNDIV module with input frequencies above 14 GHz, the PRE[:MODulus] command must be used to set the prescaler ratio to 4 or 8.

Schematic Diagram